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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,451	08/19/2003	Eric O. Zuber	02CR360/KE	4397

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ROCKWELL COLLINS, INC.  
INTELLECTUAL PROPERTY DEPARTMENT  
400 COLLINS ROAD NE  
M/S 124-323  
CEDAR RAPIDS, IA 52498

EXAMINER
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GEE, JASON KAI YIN

ART UNIT	PAPER NUMBER
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2434

MAIL DATE	DELIVERY MODE
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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/643,451	<b>Applicant(s)</b> ZUBER ET AL.	
	<b>Examiner</b> JASON K. GEE	<b>Art Unit</b> 2434	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 17-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 17-20 is/are rejected.
- 7) ☒ Claim(s) 21-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

***DETAILED ACTION***

1. This action is response to communication: RCE filed on 07/16/2009.
2. Claims 1-6 and 17-24 are currently pending in this application. Claims 1, 17, and 21 are independent claims.
3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/16/2009 has been entered.

***Response to Arguments***

4. Applicants' arguments and amendments to claim 21 have overcome the prior art or record and the rejection for that claim has been withdrawn.
5. Applicant's arguments filed 07/16/2009 in regards to claims 1 and 17 have been fully considered but are not persuasive.

As per claims 1 and 17, the applicants argue that Sherman teaches away from encoding the information to be not decodable by another processor as Sherman teaches physical isolation of processes in predefined security levels. The applicants further argue that the TCB's in Sherman assigned at a first security level can decode data that has a second security level protection. However, this is not how Sherman acts as a whole. The applicants point to col. 4 lines 45-50, wherein it recites that under

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established security rules, no information may flow between nodes of lower to higher security absent a need to know. However, this flow of information, even if it may be flowed from a lower security to a higher security, is not the decoding of encoded information at different security levels. As seen in proceeding paragraph, in col. 4 lines 60 to col. 5 line 3, each processor is restricted to processing data at the assigned security level it is associated with. Thus, even if information may flow from a processor to another processor, processors can only process data at the level it is associated with. Thus, Sherman teaches that the encoded information is not decodable by another processor corresponding to a different security level, as the processors are configured to only process information at its own security level.

### ***Claim Rejections - 35 USC § 112***

6. The previous 112 rejections have been withdrawn in response to applicants' amendments.

### ***Claim Objections***

7. Claim 21 is objected to because of the following informalities:

8. As per claim 21, the claim recites "wherein a re-encapsulated channel encrypted outbound packet being configured to be able to be decoded by processors assigned to the first security level." There are grammatical errors in this clause, and perhaps should be amended to "wherein a re-encapsulated channel encrypted outbound packet

configured to be able to be decoded by processors **is** assigned to the first security level.”

. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-4, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable Thedens et al. US Patent No. 6,041,035 (hereinafter Thedens) in view of Sherman et al. US Patent No. 5,075,884 (hereinafter Sherman).

As per claim 1, Thedens teaches a multi-channel radio operating with multiple security levels, comprising: more than one input, each input corresponding to a security level (Figure 1, with security levels of red/black); a first set of more than one processors, each of the processors in the first set of more than one processors is coupled to one of the inputs (Figure 1; also col. 5 lines 60-67, wherein there are multiple black and red processing modules, wherein processors are 262 and 282; each of the processors in the first set of more than one processors corresponding to the security level of the respective input (Figure 1; also col. 4 lines 25-38) ; a second set of processors coupled

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to the first set of more than one processors via a first common bus (Figure 1, wherein second processor is processor 302); wherein one of the processors of the first set of more than one processors encodes information received from the input to provide encoded information (col. 4 lines 25-38); wherein the encoded information is configured to be able to be decoded by devices corresponding to the security level of the one of the processors of the first set of more than one processors (col. 4 lines 25-38); wherein the first common bus is configured to direct the encoded information to an intended processor of the second set of more than one processor, the intended processor corresponding to the security level (col. 5 line 60 to col. 6 line 14).

However, at the time of the invention, Thedens does not explicitly teach a second set of more than one processors. Thedens teaches at least one processor though, as mentioned above, such as processor 302. Having additional processors is well known in the art though, such as taught by Sherman. Sherman teaches wherein systems implement multiple processors to implement multi-level security (col. 4 line 60 to col. 5 line 3). Sherman further teaches wherein the encoded information is not decodable by another processor of the second set of more than one processors corresponding to a different security level (col. 4 line 60 to col. 5 line 3, wherein each processor is dedicated to a specific security level and is restricted to only processing data at that security level).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the teachings of Sherman with Thedens. Having multiple processors for multiple security levels is well known in the art, as Sherman throughout this

applicatin. As seen, each processor is dedicated to processing information at a different level, and thus, it would make the system more secure as each processor can only perform the security level it is assigned.

As per claim 2, Thedens teaches wherein the first set of more than one processors are red processing devices (Figure 1).

As per claim 3, Thedens teaches wherein the second set of more than one processors are black processing devices (Figure 1)

As per claim 4, Thedens teaches wherein the first set of more than one processors are red processing devices (Figure 1)

Claim 17 is rejected using the same basis of arguments used to reject claim 1 above.

Claim 18 is rejected using the same basis of arguments used to reject claim 2 above.

Claim 20 is rejected using the same basis of arguments used to reject claim 3 above.

11. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thedens and Sherman as applied above, and further in view of Fletcher US SIR Reg. No. H1,836 (hereinafter Fletcher).

As per claim 5, the Thedens teaches switching devices, but does not explicitly teach wherein the first common bus is an Ethernet packet switching device. However,

using Ethernet devices are well known in the art, as pertaining to multi-channel communication radios, and are taught throughout Fletcher, such as in col. 16 lines 20-30.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the Thedens and Sherman combination with Fletcher. Fletcher teaches that a switching modules may include many components, such as busses and Ethernet interfaces. As Ethernet is well known in the art and used commonly to those in the field, it would have been obvious to make a switch compatible for Ethernet packets. Providing an Ethernet switch would make the invention more practical and adaptable to use as Ethernet is well known and used frequently.

12. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thedens and Sherman as applied above, and further in view of Mahany US Patent No. 5,960,344 (hereinafter Mahany).

As per claim 6, the Thedens combination teaches the use of a bus, but does not explicitly recite PCI busses. However, PCI busses are well known in the art, and may be implemented in multi-channel radios, such as taught by Mahany in col. 9 lines 10-21.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the Thedens combination with Mahany. PCI busses are well known in the art and used commonly, and it would have been obvious to incorporate PCI busses to make the systems compatible with the systems on the market.



Claim 19 is rejected using the same basis of arguments used to reject claim 6 above.

***Allowable Subject Matter***

13. Claims 21-24 would be allowable if rewritten to overcome the minor claim objects as set forth in the Office Action above.

The following is a statement of reasons for the indication of allowable subject matter: The applicants have amended the claims which overcome the prior art of record.

***Conclusion***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON K. GEE whose telephone number is (571)272-6431. The examiner can normally be reached on M-F, 7:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on (571) 272-3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

/Jason K Gee/  
Examiner, Art Unit 2434

/Gilberto Barron Jr./  
Supervisory Patent Examiner, Art Unit 2432